CLAIMS

1. A memory device data path, comprising:

a storage device storing N bits of data;

a first bus having N/2 bits coupled to the storage device;

a second bus having N/2 bits coupled to the storage device;

a first set of N/2M parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, the parallel-to-serial converters in the first set being operable in a first operating mode to receive from the storage device through the first bus 2 sets of parallel data each containing M bits and apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of N/2M parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, the parallel-to-serial converters in the second set being operable in the first operating mode to receive from the storage device through the second bus 2 sets of parallel data each containing M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, the parallel-to-serial converters in the second set being operable in a second operating mode to receive from the storage device through the first and second buses a set of parallel data containing 2M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

2. The memory device data path of claim 1, wherein N is equal to 32 and M is equal to 4.

3. The memory device data path of claim 1, wherein the storage device comprises N flip-flops.

4. The memory device data path of claim 1, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to one of the first and second buses to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one status signal indicative of the operating state of the first set of latches; and

a flip-flop set responsive to an initiate signal and reset responsive to a status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the control terminal to apply a shift control signal to the control terminal to allow the data bits to be shifted out of the first set of latches when the flip-flop is set.

5. The memory device data path of claim 1, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to the first bus to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a first control terminal receiving a first shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one first status signal indicative of the operating state of the first set of latches; and

a first flip-flop set responsive to an initiate signal and reset responsive to a first status signal indicating that all of the data bits stored in the first set of latches

have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the first control terminal to apply a first shift control signal to the first control terminal to allow the data bits to be shifted out of the first set of latches when the first flip-flop is set;

a second set of latches having a set of M parallel input terminals coupled to the second bus to receive and store the data bits, the second set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a second shift control signal allowing the data bits to be shifted out of the second set of latches responsive to the clock signal, and an output terminal generating at least one second status signal indicative of the operating state of the second set of latches; and

a second flip-flop set responsive to the first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches and reset responsive to a second status signal indicating that all of the data bits stored in the second set of latches have been shifted out of the second set of latches responsive to the serial clock signal, the second flip-flop having an output terminal coupled to the control terminal to apply a second shift control signal to the second control terminal to allow the data bits to be shifted out of the second set of latches when the second flip-flop is set.

6. The memory device data path of claim 1, wherein the storage device stores 2N bits of data in the first operating mode and N bits of data in the second operating mode.

7. A parallel-to-serial converter, comprising:

a first set of latches having a set of M parallel input terminals to receive and store M data bits, the first set of latches further including a serial output terminal coupled to a respective data output terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and a status output

terminal generating at least one status signal indicative of the operating state of the first set of latches; and

a flip-flop set responsive to an initiate signal and reset responsive to a status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the control terminal to apply a shift control signal to the control terminal to allow the data bits to be shifted out of the first set of latches when the flip-flop is set.

8. A parallel-to-serial converter, comprising:

a first set of latches having a set of M parallel input terminals coupled to receive and store M data bits, the first set of latches further including a serial output terminal coupled to a respective data output terminal, a serial clock terminal receiving a clock signal, a first control terminal receiving a first shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and a status output terminal generating at least one first status signal indicative of the operating state of the first set of latches; and

a first flip-flop set responsive to an initiate signal and reset responsive to a first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the first control terminal to apply a first shift control signal to the first control terminal to allow the data bits to be shifted out of the first set of latches when the first flip-flop is set;

a second set of latches having a set of M parallel input terminals coupled to receive and store M data bits, the second set of latches further including a serial output terminal coupled to a respective data output terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a second shift control signal allowing the data bits to be shifted out of the second set of latches responsive to the clock signal, and a status output terminal generating at least one second status signal indicative of the operating state of the second set of latches; and

a second flip-flop set responsive to the first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches and reset responsive to a second status signal indicating that all of the data bits stored in the second set of latches have been shifted out of the second set of latches responsive to the serial clock signal, the second flip-flop having an output terminal coupled to the control terminal to apply a second shift control signal to the second control terminal to allow the data bits to be shifted out of the second set of latches when the second flip-flop is set.

9. A memory device, comprising:

an array of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in the array;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in the array;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

a first bus coupled to receive N/2 data bits from the array;

a second bus coupled to receive N/2 data bits from the array;

a first set of N/2M parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, each of the N/2M parallel-to-serial converters in the first set being operable in a first operating mode to read 2 sets of data from the array each containing M bits, the M bits in each set being coupled through the first bus, the first set of parallel-to-serial converters further being operable in the first operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of N/2M parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, each of the N/2M parallel-to-serial converters in the second set being operable in the first operating mode to read 2 sets of data from the array each containing M bits coupled through the second bus, the second set of parallel-to-serial converters further being operable in the first operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, each of the N/2M parallel-to-serial converters in the second set being operable in a second operating mode to read a set of data from the array containing 2M bits coupled through the first and second buses, the second set of parallel-to-serial converters further being operable in the second operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

10. The memory device of claim 9, wherein N is equal to 32 and M is equal to 4.

11. The memory device of claim 9, further comprising a storage device coupled to the array, the storage device being operable to temporarily store the data bits read from the array.

12. The memory device of claim 11, wherein the storage device is operable to temporarily store N bits of data in the first operating mode and N bits of data in the second operating mode.

13. The memory device of claim 11, wherein the storage device is operable to temporarily store 2N bits of data in the first operating mode and N bits of data in the second operating mode.

14. The memory device of claim 9, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to one of the first and second buses to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one status signal indicative of the operating state of the first set of latches; and

a flip-flop set responsive to an initiate signal and reset responsive to a status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the control terminal to apply a shift control signal to the control terminal to allow the data bits to be shifted out of the first set of latches when the flip-flop is set.

15. The memory device of claim 9, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to the first bus to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a first control terminal receiving a first shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one first status signal indicative of the operating state of the first set of latches; and

a first flip-flop set responsive to an initiate signal and reset responsive to a first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the first control terminal to apply a first

shift control signal to the first control terminal to allow the data bits to be shifted out of the first set of latches when the first flip-flop is set;

a second set of latches having a set of M parallel input terminals coupled to the second bus to receive and store the data bits, the second set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a second shift control signal allowing the data bits to be shifted out of the second set of latches responsive to the clock signal, and an output terminal generating at least one second status signal indicative of the operating state of the second set of latches; and

a second flip-flop set responsive to the first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches and reset responsive to a second status signal indicating that all of the data bits stored in the second set of latches have been shifted out of the second set of latches responsive to the serial clock signal, the second flip-flop having an output terminal coupled to the control terminal to apply a second shift control signal to the second control terminal to allow the data bits to be shifted out of the second set of latches when the second flip-flop is set.

16. The memory device of claim 9, wherein the memory device comprises a dynamic random access memory.

17. The memory device of claim 16, wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

18. A memory device, comprising:

an array of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in the array;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in the array;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

a storage device operable to store 2N bits of data in a first operating mode and N bits of data in a second operating mode;

a first bus having N/2 bits coupled to the storage device;

a second bus having N/2 bits coupled to the storage device;

a first set of parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, the parallel-to-serial converters in the first set being operable in the first operating mode to receive from the storage device through the first bus 2 sets of parallel data each containing M bits and apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, the parallel-to-serial converters in the second set being operable in the first operating mode to receive from the storage device through the second bus 2 sets of parallel data each containing M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, the parallel-to-serial converters in the second set being operable in a second mode to receive from the storage device through the first and second buses a set of parallel data containing 2M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

19. The memory device of claim 18, wherein N is equal to 32 and M is equal to 4.

20. The memory device of claim 18, wherein the storage device comprises 2N flip-flops, N of which are used in the second operating mode.

21. The memory device data path of claim 18, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to one of the first and second buses to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one status signal indicative of the operating state of the first set of latches; and

a flip-flop set responsive to an initiate signal and reset responsive to a status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the control terminal to apply a shift control signal to the control terminal to allow the data bits to be shifted out of the first set of latches when the flip-flop is set.

22. The memory device of claim 18, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to the first bus to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a first control terminal receiving a first shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock

signal, and an output terminal generating at least one first status signal indicative of the operating state of the first set of latches; and

a first flip-flop set responsive to an initiate signal and reset responsive to a first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the first control terminal to apply a first shift control signal to the first control terminal to allow the data bits to be shifted out of the first set of latches when the first flip-flop is set;

a second set of latches having a set of M parallel input terminals coupled to the second bus to receive and store the data bits, the second set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a second shift control signal allowing the data bits to be shifted out of the second set of latches responsive to the clock signal, and an output terminal generating at least one second status signal indicative of the operating state of the second set of latches; and

a second flip-flop set responsive to the first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches and reset responsive to a second status signal indicating that all of the data bits stored in the second set of latches have been shifted out of the second set of latches responsive to the serial clock signal, the second flip-flop having an output terminal coupled to the control terminal to apply a second shift control signal to the second control terminal to allow the data bits to be shifted out of the second set of latches when the second flip-flop is set.

23. The memory device of claim 18, wherein the memory device comprises a dynamic random access memory.

24. The memory device of claim 23, wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

25. A memory device, comprising:

a plurality of banks of memory arrays, each of the memory arrays containing a plurality of sub-arrays arranged in rows and columns, each of the sub-arrays containing a plurality of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in one of the sub-arrays of one of the banks;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in one of the sub-arrays of one of the banks;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

P*M storage devices each operable to store a respective bits of data received from each of P corresponding columns of sub-arrays;

a first bus having M*L/2 bits coupled to P*M/2 of the storage devices;

a second bus having M*L/2 bits coupled to P*M/2 of the storage devices;

a first set of L/2 parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of L/2 respective data bus terminals, each of the L/2 parallel-to-serial converters in the first set being operable in the first operating mode to receive from the storage device through the first bus 2L/P sets of parallel data each containing M*P/L bits and apply L/2 bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of L/2 parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of L/2 respective data bus terminals, each of the L/2 parallel-to-serial converters in the second set being

operable in the first operating mode to receive from the storage device through the second bus 2L/P sets of parallel data each containing M*P/L bits and to apply L/2 bursts each containing 2M bits to respective data bus terminals in the second set, each of the L/2 parallel-to-serial converters in the second set being operable in a second mode to receive from the storage device through the first and second buses L/P sets of parallel data containing 2M*P/L bits and to apply L/2 bursts each containing 2M bits to respective data bus terminals in the second set.

26. The memory device of claim 25, wherein P is equal to 8, L is equal to 8, and M is equal to 4.

27. The memory device of claim 25, wherein l is equal to 8 and M is equal to 4, and wherein P is equal to 16 in the first operating mode and P is equal to 8 in the second operating mode.

28. The memory device of claim 25, wherein the P*M storage devices comprise P*M flip-flops.

29. The memory device data path of claim 25, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to one of the first and second buses to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one status signal indicative of the operating state of the first set of latches; and

a flip-flop set responsive to an initiate signal and reset responsive to a status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-

flop having an output terminal coupled to the control terminal to apply a shift control signal to the control terminal to allow the data bits to be shifted out of the first set of latches when the flip-flop is set.

30. The memory device of claim 25, wherein the parallel-to-serial converters comprise:

a first set of latches having a set of M parallel input terminals coupled to the first bus to receive and store the data bits, the first set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a first control terminal receiving a first shift control signal allowing the data bits to be shifted out of the first set of latches responsive to the clock signal, and an output terminal generating at least one first status signal indicative of the operating state of the first set of latches; and

a first flip-flop set responsive to an initiate signal and reset responsive to a first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches responsive to the serial clock signal, the flip-flop having an output terminal coupled to the first control terminal to apply a first shift control signal to the first control terminal to allow the data bits to be shifted out of the first set of latches when the first flip-flop is set;

a second set of latches having a set of M parallel input terminals coupled to the second bus to receive and store the data bits, the second set of latches further including a serial output terminal coupled to a respective data bus terminal, a serial clock terminal receiving a clock signal, a control terminal receiving a second shift control signal allowing the data bits to be shifted out of the second set of latches responsive to the clock signal, and an output terminal generating at least one second status signal indicative of the operating state of the second set of latches; and

a second flip-flop set responsive to the first status signal indicating that all of the data bits stored in the first set of latches have been shifted out of the first set of latches and reset responsive to a second status signal indicating that all of the data bits stored in the second set of latches have been shifted out of the second set of

latches responsive to the serial clock signal, the second flip-flop having an output terminal coupled to the control terminal to apply a second shift control signal to the second control terminal to allow the data bits to be shifted out of the second set of latches when the second flip-flop is set.

31. The memory device of claim 25, wherein the memory device comprises a dynamic random access memory.

32. The memory device of claim 31, wherein the dynamic random access memory comprises a synchronous dynamic random access memory.

33. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in the array;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in the array;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

a first bus coupled to receive N/2 data bits from the array;

a second bus coupled to receive N/2 data bits from the array;

a first set of N/2M parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input

terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, each of the N/2M parallel-to-serial converters in the first set being operable in a first operating mode to read 2 sets of data from the array each containing M bits, the M bits in each set being coupled through the first bus, the first set of parallel-to-serial converters further being operable in the first operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of N/2M parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, each of the N/2M parallel-to-serial converters in the second set being operable in the first operating mode to read 2 sets of data from the array each containing M bits coupled through the second bus, the second set of parallel-to-serial converters further being operable in the first operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, each of the N/2M parallel-to-serial converters in the second set being operable in a second operating mode to read a set of data from the array containing 2M bits coupled through the first and second buses, the second set of parallel-to-serial converters further being operable in the second operating mode to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

34. The computer system of claim 33, wherein N is equal to 32 and M is equal to 4.

35. The computer system of claim 33, further comprising a storage device coupled to the array, the storage device being operable to temporarily store the data bits read from the array.

36. The computer system of claim 35, wherein the storage device is operable to temporarily store N bits of data in the first operating mode and N bits of data in the second operating mode.

37. The computer system of claim 35, wherein the storage device is operable to temporarily store 2N bits of data in the first operating mode and N bits of data in the second operating mode.

38. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory, comprising:

an array of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in the array;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in the array;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

a storage device operable to store 2N bits of data in a first operating mode and N bits of data in a second operating mode;

a first bus having N/2 bits coupled to the storage device;

a second bus having N/2 bits coupled to the storage device;

a first set of parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of N/2M respective data bus terminals, the parallel-to-serial converters in the first set being operable in the first operating mode to receive from the storage device through the first bus 2 sets of parallel data each containing M bits and apply N/2M bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of N/2M respective data bus terminals, the parallel-to-serial converters in the second set being operable in the first operating mode to receive from the storage device through the second bus 2 sets of parallel data each containing M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set, the parallel-to-serial converters in the second set being operable in a second mode to receive from the storage device through the first and second buses a set of parallel data containing 2M bits and to apply N/2M bursts each containing 2M bits to respective data bus terminals in the second set.

39. The computer system of claim 38, wherein N is equal to 32 and M is equal to 4.

40. The computer system of claim 38, wherein the storage device comprises 2N flip-flops, N of which are used in the second operating mode.

41. A computer system, comprising:

computer circuitry operable to perform computing functions;

at least one input device coupled to the computer circuitry;

at least one output device coupled to the computer circuitry;

at least one data storage devices coupled to the computer circuitry; and

a dynamic random access memory, comprising:

a plurality of banks of memory arrays, each of the memory arrays containing a plurality of sub-arrays arranged in rows and columns, each of the sub-arrays containing a plurality of memory cells arranged in rows and columns;

a row address decoder coupled to receive a row address signal and to enable a corresponding row of memory cells in one of the sub-arrays of one of the banks;

a column address decoder coupled to receive a column address signal and to enable a corresponding column of memory cells in one of the sub-arrays of one of the banks;

a command decoder operable to receive memory commands from a command bus and to generate control signals corresponding to respective memory commands; and

a read data path, comprising:

P*M storage devices each operable to store a respective bits of data received from each of P corresponding columns of sub-arrays;

a first bus having M*L/2 bits coupled to P*M/2 of the storage devices;

a second bus having M*L/2 bits coupled to P*M/2 of the storage devices;

a first set of L/2 parallel-to-serial converters coupled to the first bus, each of the parallel-to-serial converters in the first set having M input terminals coupled to receive M respective bits from the first bus, the parallel-to-serial converters in the first set having respective serial output terminals coupled to a first set of L/2 respective data bus terminals, each of the L/2

parallel-to-serial converters in the first set being operable in the first operating mode to receive from the storage device through the first bus 2L/P sets of parallel data each containing M*P/L bits and apply L/2 bursts each containing 2M bits to respective data bus terminals in the first set; and

a second set of L/2 parallel-to-serial converters coupled to the first and second buses, each of the parallel-to-serial converters in the second set having M input terminals coupled to receive M respective bits from the first bus and M respective bits from the second bus, the parallel-to-serial converters in the second set having respective serial output terminals coupled to a second set of L/2 respective data bus terminals, each of the L/2 parallel-to-serial converters in the second set being operable in the first operating mode to receive from the storage device through the second bus 2L/P sets of parallel data each containing M*P/L bits and to apply L/2 bursts each containing 2M bits to respective data bus terminals in the second set, each of the L/2 parallel-to-serial converters in the second set being operable in a second mode to receive from the storage device through the first and second buses L/P sets of parallel data containing 2M*P/L bits and to apply L/2 bursts each containing 2M bits to respective data bus terminals in the second set.

42. The computer system of claim 41, wherein P is equal to 8, L is equal to 8, and M is equal to 4.

43. The computer system of claim 41, wherein l is equal to 8 and M is equal to 4, and wherein P is equal to 16 in the first operating mode and P is equal to 8 in the second operating mode.

44. The computer system of claim 41, wherein the P*M storage devices comprise P*M flip-flops.

45. A method of transferring data from a memory array in either a first operating mode or a second operating mode, the method comprising:

prefetching a first set of 2N data bits in the first operating mode;

prefetching a second set of N data bits in the second operating mode;

in the first operating mode, transferring the first set of 2N data bits to 2M data bus terminals in respective bursts of N/M bits; and

in the second operating mode, transferring the second set of data bits to M data bus terminals in M busts of N/M bits.

46. The method of claim 45, wherein the act of prefetching a first set of 2N data bits comprises:

prefetching N data bits from the memory array in a first read operation; and

prefetching N data bits from the memory array in a second read operation.

47. The method of claim 45, wherein the act of prefetching a first set of 2N data bits comprises prefetching 2N data bits from the memory array in a single read operation

48. The method of claim 45, wherein the act of transferring the first set of data bits to 2M data bus terminals in respective bursts of N/M bits in the first operating mode comprises:

transferring a first set of N parallel data bits;

transferring a second set of N parallel data bits;

converting the 2N transferred data bits to 2M bursts each containing N/M bits; and

coupling each of the 2M bursts to are respective data bus terminal.

49. The method of claim 45, wherein N is equal to 32 and M is equal to 4.

50. The method of claim 45, wherein the act of transferring the first set of data bits to 2M data bus terminals in respective bursts of N/M bits in the first operating mode comprises:

transferring each data bit in the first set of N parallel data bits from the memory array to respective first storage devices;

transferring each data bit in the second set of N parallel data bits from the memory array to respective second storage devices;

transferring the N data bits in the first storage devices to 2M parallel-to-serial converters;

transferring the N data bits in the second storage devices to the 2M parallel-to-serial converters;

using the 2M parallel-to-serial converters to convert the 2N transferred data bits to 2M bursts of serial data each containing N/M bits; and

applying the 2M bursts to respective data bus terminals.

51. A method of coupling data from a memory array to data bus terminals, comprising:

transferring from an array 2N bits of data in a first operating mode and N bits of data in a second operating mode, the data being transferred through X sets of buses each having a width of M bits;

converting the transferred parallel data to serial data; and

applying respective bursts of serial data to 2Y data bus terminals in a first mode and Y data bus terminals in a second mode, each of the bursts containing N/Y bits.

52. The method of claim 51, wherein the act of transferring the data bits from the array comprises transferring the data bits through N/M sets of buses each having a width of M bits.

53. The method of claim 51, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises:

transferring N data bits from the memory array in a first read operation; and

transferring N data bits from the memory array in a second read operation.

54. The method of claim 51, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises transferring 2N data bits from the memory array in a single read operation.

55. The method of claim 51, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises:

transferring N data bits from the memory array to a first storage device in a first read operation;

transferring N data bits from the memory array to a second storage device in a second read operation;

transferring the 2N bits of information from the first and second storage devices.

56. The method of claim 55, wherein the act of transferring 2N bits of data from the from the first and second storage devices comprises:

transferring N data bits from the first storage device through an N-bit bus; and

transferring N data bits from the second storage device through the N-bit bus.

57. The method of claim 51, wherein N is equal to 32, M is equal to 4, and Y is equal to 4.

58. The method of claim 51, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

transferring N data bits from the memory array in a first read operation in the first operating mode; and

transferring N data bits from the memory array in a second read operation in the first operating mode; and

transferring N data bits from the memory array in a first read operation in the second operating mode.

59. The method of claim 51, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

transferring 2N data bits from the memory array in a first read operation in the first operating mode; and

transferring N data bits from the memory array in a first read operation in the second operating mode.

60. The method of claim 51, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

in the first operating mode, transferring a first set of N data bits from the memory array to a storage device in a first read operation;

in the first operating mode, transferring the N data bits in the first set from the storage device;

in the first operating mode, transferring a second set of N data bits from the memory array to the storage device in a second read operation;

in the second operating mode, transferring a first set of N data bits from the memory array to a storage device in a first read operation; and

in the first operating mode, transferring the N data bits in the first set from the storage device.

61. The method of claim 51, wherein the act of transferring the first set of data bits to 2M data bus terminals in respective bursts of N/M bits in the first operating mode comprises:

transferring each data bit in the first set of N parallel data bits from the memory array to respective first storage devices;

transferring each data bit in the second set of N parallel data bits from the memory array to respective second storage devices;

transferring the N data bits in the first storage devices to 2M parallel-to-serial converters;

transferring the N data bits in the second storage devices to the 2M parallel-to-serial converters;

using the 2M parallel-to-serial converters to convert the 2N transferred data bits to 2M bursts of serial data each containing N/M bits; and

applying the 2M bursts to respective data bus terminals.

62. A method of coupling data from a memory array to data bus terminals, comprising:

transferring from an array 2N bits of parallel data in a first mode and N bits of parallel data in a second mode, the parallel data being transferred from the array using a bus having a width N;

converting the transferred parallel data to serial data; and

applying respective bursts of serial data to 2M data bus terminals in a first mode and M data bus terminals in a second mode, each of the bursts containing N/M bits.

63. The method of claim 62, wherein the act of transferring the data bits from the array comprises transferring the data bits through N/M sets of buses each having a width of M bits.

64. The method of claim 62, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises:

transferring N data bits from the memory array in a first read operation; and

transferring N data bits from the memory array in a second read operation.

65. The method of claim 62, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises transferring 2N data bits from the memory array in a single read operation.

66. The method of claim 62, wherein the act of transferring 2N bits of data from the array in the first operating mode comprises:

transferring N data bits from the memory array to a first storage device in a first read operation;

transferring N data bits from the memory array to a second storage device in a second read operation;

transferring the 2N bits of information from the first and second storage devices.

67. The method of claim 62, wherein the act of transferring 2N bits of data from the from the first and second storage devices comprises:

transferring N data bits from the first storage device through an N-bit bus; and

transferring N data bits from the second storage device through the N-bit bus.

68. The method of claim 62, wherein N is equal to 32 and M is equal to 4.

69. The method of claim 62, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

transferring N data bits from the memory array in a first read operation in the first operating mode; and

transferring N data bits from the memory array in a second read operation in the first operating mode; and

transferring N data bits from the memory array in a first read operation in the second operating mode.

70. The method of claim 62, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

transferring 2N data bits from the memory array in a first read operation in the first operating mode; and

transferring N data bits from the memory array in a first read operation in the second operating mode.

71. The method of claim 62, wherein the acts of transferring 2N bits of data from the array in the first operating mode and transferring N bits of information in the second operating mode comprise:

in the first operating mode, transferring a first set of N data bits from the memory array to a storage device in a first read operation;

in the first operating mode, transferring the N data bits in the first set from the storage device;

in the first operating mode, transferring a second set of N data bits from the memory array to the storage device in a second read operation;

in the second operating mode, transferring a first set of N data bits from the memory array to a storage device in a first read operation; and

in the first operating mode, transferring the N data bits in the first set from the storage device.

72. The method of claim 62, wherein the act of transferring the first set of data bits to 2M data bus terminals in respective bursts of N/M bits in the first operating mode comprises:

transferring each data bit in the first set of N parallel data bits from the memory array to respective first storage devices;

transferring each data bit in the second set of N parallel data bits from the memory array to respective second storage devices;

transferring the N data bits in the first storage devices to 2M parallel-to-serial converters;

transferring the N data bits in the second storage devices to the 2M parallel-to-serial converters;

using the 2M parallel-to-serial converters to convert the 2N transferred data bits to 2M bursts of serial data each containing N/M bits; and

applying the 2M bursts to respective data bus terminals.